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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/656,596	09/05/2003	Wing K. Luk	YOR920030119US1	7956

24299 7590 10/14/2005

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EXAMINER	
YOHA, CONNIE C	

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 10/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/656,596	LUK ET AL.	
	Examiner	Art Unit	
	Connie C. Yoha	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9,11,12,14-18,20,21 and 23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9,11,12,14-18,20,21 and 23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Connie C. Yoha

CONNIE C. YOHA
PRIMARY EXAMINER

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. The Amendment filed on 6/28/05 has been entered and are made of record.

2. Claims 1-9, 11-12, 14-18, 20-21, and 23 are pending.

Response to Arguments

3 Applicant's argument filed 5/24/00 has been fully considered.

The rejection under 35 U.S. 112 is now withdrawn.

Claim 10-12 and 22 that were objected to as containing allowable subject matter are now being withdrawn.

EXAMINER'S AMENDMENT

4. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Mr. George Sai-Halasz on 9/29/05.

The application has been amended as follows:

In claim 9 and 21 restore all canceled limitations in amended claim 9 and 21. For example, claim 9 and 21 should be as following:

9. (currently amended) A DRAM, comprising: a single ended bitline structure, wherein the DRAM has bitlines; **a plurality of primary sense amplifiers operationally engaging the bitlines and the global bitlines, wherein the primary sense amplifiers have data storage and data write-back capability, and wherein the primary sense amplifiers are being capable to decouple from the global bitlines;** a full-wordline I/O structure comprising a reduced address space, wherein the reduced address space has no column address; **wherein essentially all memory cell that are simultaneously turned on by any one wordline are being operated on by associated sense amplifiers of the primary sense amplifiers; wherein the DRAM has memory cells and wordlines;** a pipelined architecture, wherein the DRAM is functioning in cycles and in each of the cycles an operation can be initiated, and; wherein the pipelined architecture comprise synchronized operations of the single ended bitline structure, of said single ended global bitline structure, **of the primary sense amplifiers,** and of the full-wordline I/O structure.

21. (currently amended) A processor, comprising: at least one embedded DRAM macro, wherein the at least one embedded DRAM macro is further comprising: a single ended bitline structure, wherein the DRAM has bitlines; a single ended global bitline structure, wherein the DRAM has global bitlines; **a plurality of primary sense amplifiers operationally engaging the bitlines and the global bitlines, wherein the primary sense amplifiers have data storage and data write-back capability, and wherein the primary sense amplifiers are being capable to decouple from the global bitlines;** a full-wordline I/O structure comprising a reduced address space, wherein the reduced address space has no column address; **wherein**

essentially all memory cell that are simultaneously turned on by any one wordline are being operated on by associated sense amplifiers of the primary sense amplifiers; wherein the DRAM has memory cells and wordlines; a pipelined architecture, wherein the DRAM is functioning in cycles and in each of the cycles an operation can be initiated, and; wherein the pipelined architecture comprise synchronized operations of the single ended bitline structure, of said single ended global bitline structure, **the primary sense amplifiers,** and of the full-wordline I/O structure.

Claim Rejections - 35 USC ∋ 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 1-9, 11-12, 14-18, 20-21, and 23 are rejected under 35 U.S.C. 102(e as being anticipated by Luk et al, Pat. No. 6768692.

With regard to claim 1, Luk discloses a DRAM comprising: at least one primary sense amplifiers (fig. 1A, 150), wherein the least one primary sense amplifier has single ended sensing, has data storage and data write-back capability, and has at least two amplification stages (col. 1, line 25-45); and a plurality of storage cells (fig. 1A, DRAM array 100) and inherent plurality of bitlines, with a single ended bitline structure, wherein one storage cell of the plurality of storage cells and the at least one primary sense amplifier are connected by one single bitline of the plurality of bitlines (col. 1, line 30-32).

With regard to claim 2, Luk discloses further a plurality of secondary sense amplifiers (fig. 1A, 140) and a plurality of global bitlines, with a single ended global bitline structure, wherein the at least one primary sense amplifier and one secondary sense amplifier of the plurality of secondary sense amplifiers are connected by one single global line bitline of the plurality of global bitlines (col. 1, line 32-45) (also with regard to claim 4 and 5).

With regard to claim 3, Luk discloses wherein the DRAM further comprises an inherent small voltage swing design.

With regard to claim 6, Luk discloses wherein at least one primary sense amplifier comprises MOS devices, and wherein at least one of the MOS devices ahs a customized threshold (fig. 3) (also with regard to claim 7).

With regard to claim 8, Luk discloses wherein the DRAM is an embedded DRAM (fig. 1A, DRAM) (also with regard to claim 20).

With regard to claim 9 and 21, Luk discloses A DRAM, comprising: a single ended bitline structure, wherein the DRAM has bitlines (fig. 2B, local bitline 210 and Global bitline 200); a plurality of primary sense amplifiers (fig. 2A, 120) operationally engaging the bitlines (fig. 2B, 210) and the global bitlines (fig. 2B, 200), wherein the primary sense amplifiers have data storage and data write-back capability (col. 5, line 43-48), and wherein the primary sense amplifiers are being capable to decouple from the global bitlines (col. 4, line 63-col. 4); a full-wordline I/O structure comprising a reduced address space, wherein the reduced address space has no column address; wherein essentially all memory cell that are simultaneously turned on by any one wordline are being operated on by associated sense amplifiers of the primary sense

amplifiers (col. 5, line 7-8, disclosed only one word-line are active at a given time); wherein the DRAM has memory cells and wordlines (fig. 3, WL 220); a pipelined architecture, wherein the DRAM is functioning in cycles and in each of the cycles an operation can be initiated, and; wherein the pipelined architecture comprise synchronized operations of the single ended bitline structure, of said single ended global bitline structure, of the primary sense amplifiers, and of the full-wordline I/O structure (col. 6, line 5-30) (also with regard to claim 15-17).

With regard to claim 11, Luk discloses wherein a read command and a subsequent writeback command are executed in differeing cycles of the cycles (col. 6, line 13-16).

With regard to claim 12, Luk discloses wherein a read command and a subsequent writeback command are executed in a single cycles of the cycles (col. 6, line 23-25) (also with regard to claim 14).

With regard to claim 14, Luk discloses wherein a read command and a write command are executed simultaneously in a single one of the cycles (col. 5,line 58-col. 6, line 12).

With regard to claim 18 and 23, Luk discloses the DRAM is further comprises an inherent small voltage swing design.

Claim Rejections - 35 USC ∋ 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 1 are rejected under 35 U.S.C. 102(e as being anticipated by Wang et al, Pat. No. 6014338.

With regard to claim 1, Wang discloses a DRAM comprising: at least one primary sense amplifiers (fig. 1, 18), wherein the least one primary sense amplifier has single ended sensing, has data storage and data write-back capability (col. 2, line 34-44, having a feedback loop), and has at least two amplification stages (col. 2, line 17-44); and a plurality of storage cells (fig. 1, 12) and a plurality of bitlines (fig. 1, 16), with a single ended bitline structure (col. 1, line 14-15), wherein one storage cell of the plurality of storage cells and the at least one primary sense amplifier are connected by one single bitline of the plurality of bitlines (col. 2, line 63-col. 3, line 18).

With regard to claim 2, Wang discloses further a plurality of secondary sense amplifiers (fig. 1, 22) and a plurality of global bitlines (fig. 1, GBL), with a single ended global bitline structure, wherein the at least one primary sense amplifier and one secondary sense amplifier of the plurality of secondary sense amplifiers are connected by one single global line bitline of the plurality of global bitlines (col. 2, line 17-44) (also with regard to claim 4 and 5).

With regard to claim 3, Wang discloses wherein the DRAM further comprises an inherent small voltage swing design.

With regard to claim 6, Wang discloses wherein at least one primary sense amplifier comprises MOS devices, and wherein at least one of the MOS devices ahs a customized threshold (fig. 2 and 3) (also with regard to claim 7).

With regard to claim 8, Wang Luk discloses wherein the DRAM is an embedded DRAM (col. 3, line 19-26).

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to whose telephone number is (571) 272-1799. The examiner can normally be reached on Mon. - Fri. from 8:00 A.M. to 5:30 PM. The examiner's supervisor, David Nelms, can be reached at (571) 272-1787. The fax phone number for this Group is (703) 872-9306. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-0956.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov should you have questions on access to the Private Pair system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

C.Yoha

September 2005

CONNIE C. YOHA
PRIMARY EXAMINER